CLAIMS IN CURRENT FORM

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (PREVIOUSLY PRESENTED) An apparatus comprising:

a circuit configured to (i) generate an output having a frequency and (ii) adjust said frequency in response to a measured duration of a known time interval associated with a predefined bit pattern occurring in an input data stream.

2. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said input data stream comprises one or more of said time intervals.

3. (PREVIOUSLY PRESENTED) The apparatus according to claim 2, wherein said time intervals are delimited by periodic events in said input data stream.

4. (PREVIOUSLY PRESENTED) The apparatus according to claim 3, wherein said periodic events comprise start-of-frame (SOF) packets of a Universal Serial Bus (USB) protocol.

5. (ORIGINAL) The apparatus according to claim 1, wherein said frequency is adjusted to within 0.25% of a host data rate.

6. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said circuit comprises:

a calibration circuit configured to generate a control signal in response to said input data stream and said output; and

an oscillator circuit configured to generate said output in response to said control signal.

7. (PREVIOUSLY PRESENTED) The apparatus according to claim 6, wherein said oscillator circuit is digitally tunable.

8. (PREVIOUSLY PRESENTED) The apparatus according to claim 6, wherein said calibration circuit comprises a detector circuit configured to detect said predefined bit pattern.

9. (PREVIOUSLY PRESENTED) The apparatus according to claim 8, wherein said detector circuit is further configured to detect a SOF packet.

10. (ORIGINAL) The apparatus according to claim 6, wherein said calibration circuit comprises one or more counters.

11. (ORIGINAL) The apparatus according to claim 10, wherein said counters are configured to start counting in response to a first SOF packet and stop counting in response to a second SOF packet.

12. (ORIGINAL) The apparatus according to claim 10, wherein said counters are configured to count in response to said output.

13. (ORIGINAL) The apparatus according to claim 6, wherein said calibration circuit comprises a look-up table.

14. (ORIGINAL) The apparatus according to claim 13, wherein said look-up table contains a number of values for adjusting said frequency.

15. (PREVIOUSLY PRESENTED) An apparatus comprising:

means for generating an output having a frequency;

means for measuring a known time interval between occurrences of a predefined bit pattern in an input using said output; and

means for adjusting said generating means in response to said measurement.

16. (PREVIOUSLY PRESENTED) A method for providing a precise clock using a precisely known time interval having a known precise duration of a data stream comprising the steps of:

(A) measuring the known time interval between occurrences of a predefined bit pattern in said data stream using said clock; and

(B) adjusting said clock in response to a difference between said measurement and said known duration.

17. (ORIGINAL) The method according to claim 16, wherein said time interval comprises the time between a pair of SOF packets.

18. (PREVIOUSLY PRESENTED) The method according to claim 16, wherein the step A comprises the sub-steps of:

(A-1) starting a counter in response to a first occurrence of said predefined bit pattern that starts said known time interval;

(A-2) counting in response to said clock; and

(A-3) stopping said counter in response to a second occurrence of said predefined bit pattern that ends said known time interval.

19. (PREVIOUSLY PRESENTED) The method according to claim 16, wherein the step B comprises the sub-steps of:

(B-1) comparing a measurement of said known time interval between occurrences of said predefined bit pattern with the known duration of said known time interval;

(B-2) retrieving a correction value from a look-up table addressed using a difference between said measurement and said known duration; and

(B-3) presenting said correction value to a digitally tunable oscillator.

20. (PREVIOUSLY PRESENTED) The method according to claim 16, wherein the step B comprises the sub-steps of:

(B-1) starting a counter in response to a first occurrence of said predefined bit pattern that starts said known time interval;

(B-2) computing a correction value using said difference between said measurement and said known duration; and

(B-3) presenting said correction value to a digitally tunable oscillator.

21. (PREVIOUSLY PRESENTED) The method according to claim 16, wherein the measured time interval comprises a plurality of SOF packets.

22. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said predefined bit pattern comprises a packet identifier field of a SOF packet.

23. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said circuit comprises:

a detector circuit configured to generate a detection signal in response to detecting said predefined bit pattern in said input data stream; and

a counter circuit configured to generate a count signal in response to said detection signal and said output.

24. (PREVIOUSLY PRESENTED) The apparatus according to claim 23, wherein said circuit further comprises:

a control circuit configured to generate a tuning signal in response to said count signal and said output; and

an oscillator circuit configured to generate said output in response to said tuning signal.

25. (PREVIOUSLY PRESENTED) The apparatus according to claim 4, wherein said input data stream comprises USB 2.0 host full-speed communications SOF packets.